A 20GHz SILICON MICROWAVE MONOLITHIC INTEGRATED CIRCUITS PROCESS AND A 7.4GHz FREQUENCY DIVIDER

*Shinichi MIYAZAKI, *Chizuko TAKAI, *Kouhei EGUCHI and +Takaaki NAKATA

*Consumer LSI Division, +Compound Semiconductor Device Division,
NEC Corporation, Kawasaki, Japan

Abstract

A Silicon Microwave Monolithic Integrated Circuits process named "DNP-Ⅲ" has been developed without self-alignment technique. By using "DNP-Ⅲ" process, NPN transistors with 0.6um width and 0.1um depth emitter achieved f_T of 20GHz. Maximum dividing frequency (Fmax) of 7.4GHz at Vcc=6V was also achieved for 1/2 prescaler with master slave T-type flip-flop.

I. Introduction

In recent years,Si bipolar transistors operating at microwave frequencies have been developed(1,2). A 10GHz frequency divider using self-aligned transistor structures called "SST-1B" (f_T=27GHz) was reported(1). A 4GHz light transmission ICs (Integrated Circuits) was also realized using self-aligned transistors called "ESPER" (f_T=12GHz)(2). However, those devices had many difficulties in fabrication processes because complicated self-alignment techniques were used.

We have already reported a f_T=10GHz Silicon Microwave Monolithic Integrated Circuits (Si-MMIC) process without self-aligned structures called "DNP(Direct Nitride Passivated base surface)-Ⅱ" and its application to a 2.6GHz wide band amplifier(3).

In this paper, we demonstrate a newly developed f_T=20GHz Si-MMIC process named "DNP-Ⅲ" with 0.1um depth and 0.6um width emitter. We also demonstrate a 7.4GHz frequency divider using "DNP-Ⅲ" process.

II. Process design

Figure 1 shows a schematic cross section of an NPN transistor and a poly-Si resistor. "DNP-Ⅲ" process design is as follows.

1. Using high resolution photolithography technique, 0.6um width fine emitter stripe can be realized to reduce base resistance (rbb') and parasitic capacitance (Cebo,Ccbo etc.) of the transistors.
2. Arsenic ion implanted buried layer and thin epitaxial layer with low resistivity reduce collector resistance.

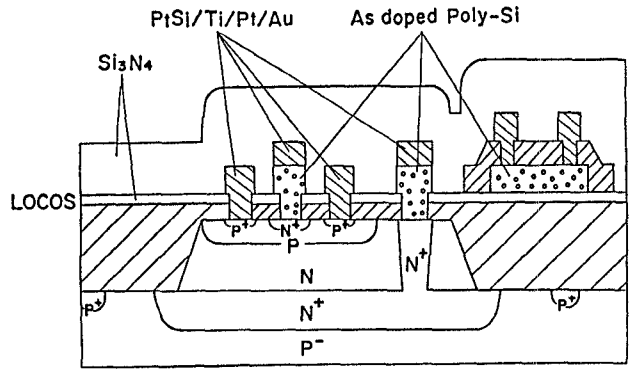

Figure 1. A schematic cross section of an NPN Transistor and poly-Si resistor in "DNP-Ⅲ" process.

3. Low energy boron ion implantation forms 0.2um depth base junction. Arsenic ions implantated into poly-Si make 0.1um depth emitter. Therefore base transition time delay (τb) is reduced to a half value of conventional process.
4. Si_3N_4 passivation assures high reliability.
5. PtSi/Ti/Pt/Au metallization and RIE process are adopted. Highly reliable 1.0um line and space electrode can be achieved.
6. Arsenic ion implanted poly-Si resistor on thick Silicon oxide(LOCOS) has 220Ω/□ sheet resistance and low parasitic capacitance. Therefore, good electrical performances of the IC's are expected in microwave frequency range.

In addition, the selectively ion implanted collector (SIC) technique(1) was used in "DNP-Ⅲ" process to achieve higher cut off frequency of the NPN transistor.

"SIC" process technique is as follows.

7. Phosphorus ions are implanted at base-collector junction beneath the emitter. The lightly doped N type region between base and epitaxial layer can suppress Kirk-effect and narrow the base width.

Figure 2 shows a microphotograph of the NPN transistor (Emitter size is 0.6um X 20um), and Fig.3 shows a SEM photograph of cross section for the NPN transistor.

CH2725-0/89/0000-1065$01.00 © 1989 IEEE

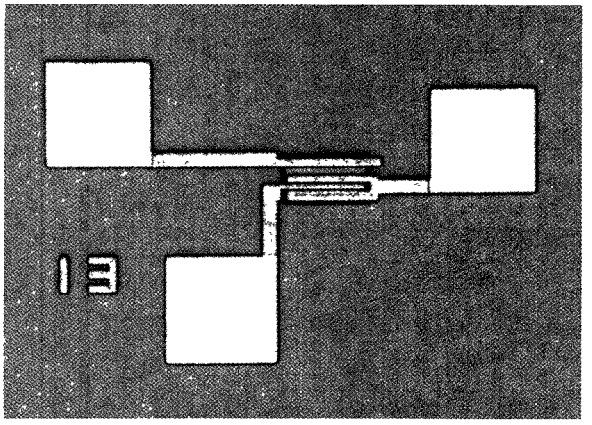

Figure 2. A microphotograph of the NPN transistor.
(Emitter size is 0.6um X 20um)

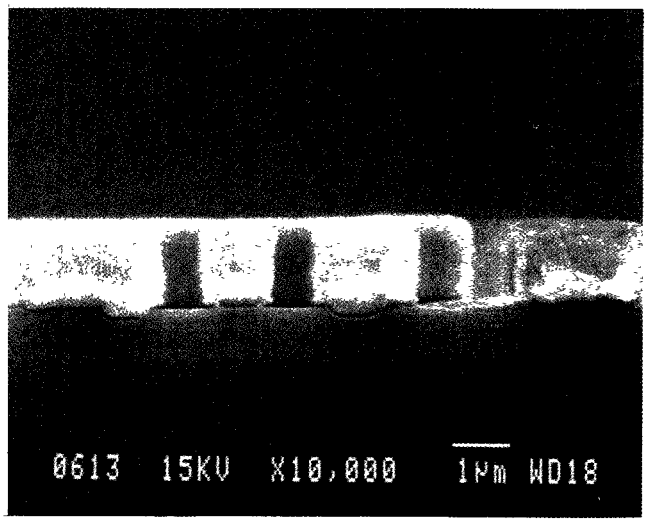

Figure 3. A SEM photograph of cross section for the NPN transistor.

III.Electrical Characteristics

S-parameters were measured for NPN transistors with 0.6um X 40um emitter, double base and single collector.

A HP-8510A network analyzer and on-wafer probing system were used calibrating an open, short and through on wafer patterns. Only 50Ω load was calibrated on 50Ω load chip. Therefore, parasitic capacitance and inductance were eliminated in this measurement.

Figure 4 shows f_T and $|S_{21e}|^2$ characteristics as a function of collector current (Ic) for an NPN transistor with 0.6um X 40um emitter. A f_T and $|S_{21e}|^2$ were 20GHz and 16.4dB, respectively at Vce of 3V (measuring frequency is 2GHz) and Ic=10mA. At Vce of 5V, f_T of 22GHz and $|S_{21e}|^2$ of 17.1dB were achieved.

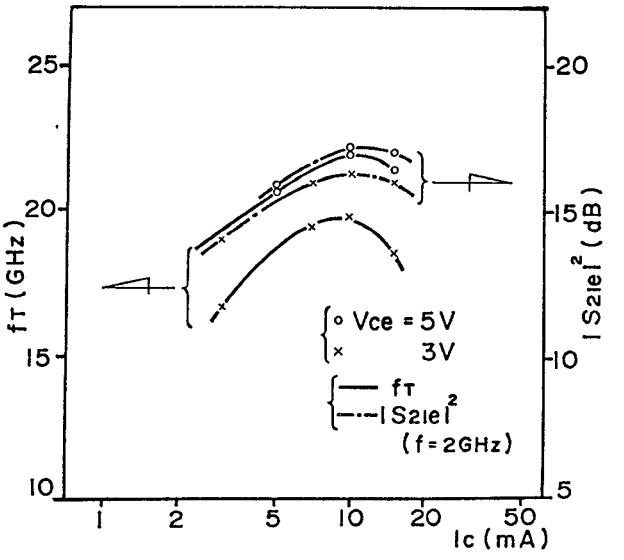

Figure 4. f_T and $|S_{21e}|^2$ characteristics as a function of collector current (Ic) for an NPN transistor with 0.6um X 40um emitter.

Electrical characteristics and device parameters are summarized in Table 1 for the transistor with 0.6um X 40um emitter. BVcbo, BVebo and BVceo were 17V, 4.5V and 6V respectively. BVceo of 6V is large enough to use ICs at supply voltage of 5V.

Table 1. Electrical characteristics and the device parameters of an NPN transistor in "DNP-Ⅲ" process.

BVcbo	17V
BVceo	6V
BVebo	4.5V
hFE	80
f_T	20GHz
$\|S_{21e}\|^2$	16.4dB
rbb'	55Ω
Cebo	0.12pF
Ccbo	0.14pF
Ccso	0.16pF

(Emitter size is 0.6μm×40μm)

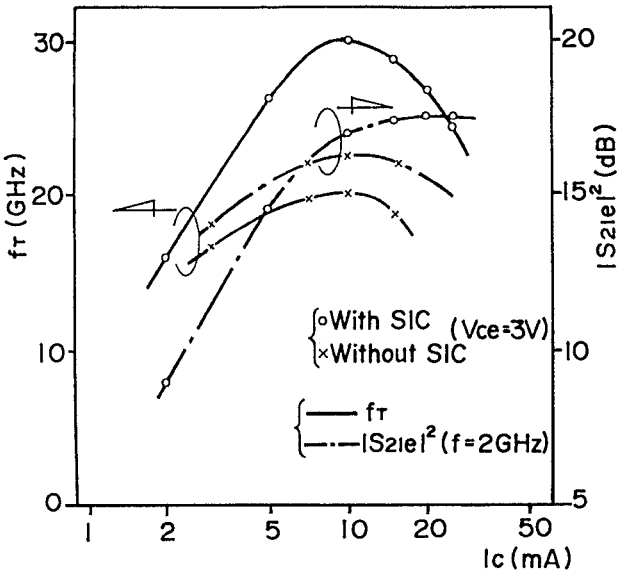

Figure 5. The difference of f_T and $|S_{21e}|^2$ characteristics for an NPN transistor between with "SIC" and without "SIC". (Emitter size is 0.6um X 40um)

Table 2. Electrical characteristics for an NPN transistor with "SIC" and without "SIC".

	Without SIC	With SIC
BVcbo	17V	7V
BVceo	6V	3.3V
BVebo	4.5V	4.1V
h_{FE}	80	120
f_T	20GHz	30GHz
$\|S_{21e}\|^2$ (f=2GHz)	16.4dB	17.5dB

(Emitter size is 0.6μm×40μm)

In addition, Fig.5 shows f_T and $|S_{21e}|^2$ characterictics for NPN transistors formed by the "SIC" technique. The f_T of 30GHz and $|S_{21e}|^2$ of 17.5dB were achieved at Vce of 3V. Figure 5 shows also the difference of f_T and $|S_{21e}|^2$ between the NPN transistors with "SIC" and without "SIC". A f_T of 10GHz and $|S_{21e}|^2$ of 1.1dB were improved for the transistor with "SIC".

However, breakdown voltages such as BVcbo and BVceo for the NPN transistor with "SIC" are lower than those for the NPN transistor of "DNP-Ⅲ" process. Table 2 shows the summary of electrical characteristics for NPN transistors with "SIC" and without "SIC". The NPN transistor with "SIC" has BVcbo of 7V and BVceo of 3.3V.

The reasons for these electrical characteristics for transistors with "SIC" are as follows.

1. Lightly doped N region in an transistor with "SIC" narrows the intrinsic base width, so that base transition time delay (τb) is reduced. At the same time, the depletion layer at the base-collector junction becomes thin so that depletion layer transition time delay(τx) reduced.

2. On the other hand, the thin depletion layer at the base-colletor junction causes avalanche breakdown at lower voltage. Consequently, it is important to use ICs with "SIC" in "DNP-Ⅲ" process below supply voltage Vcc of 3V.

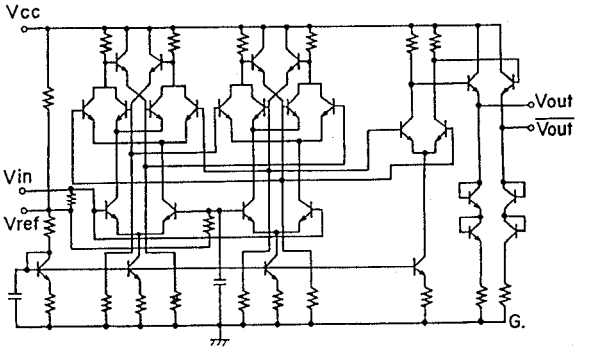

Figure 6. Equivalent circuit of 1/2 prescaler with master slave T-type flip-flop.

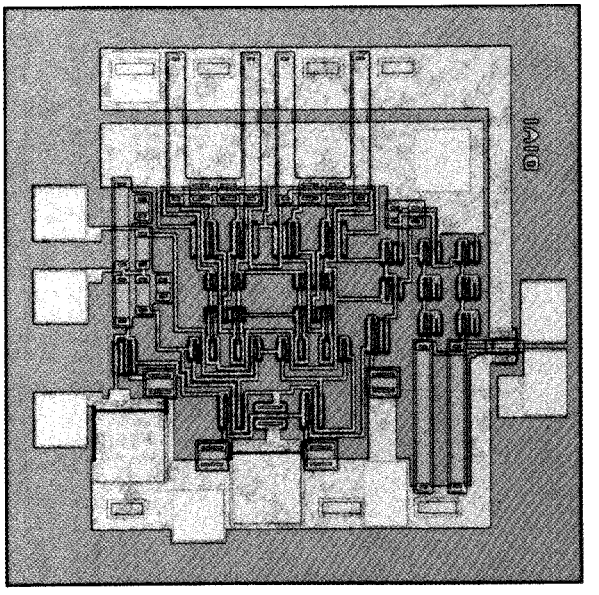

Figure 7. A microphotograph of 1/2 prescaler chip.

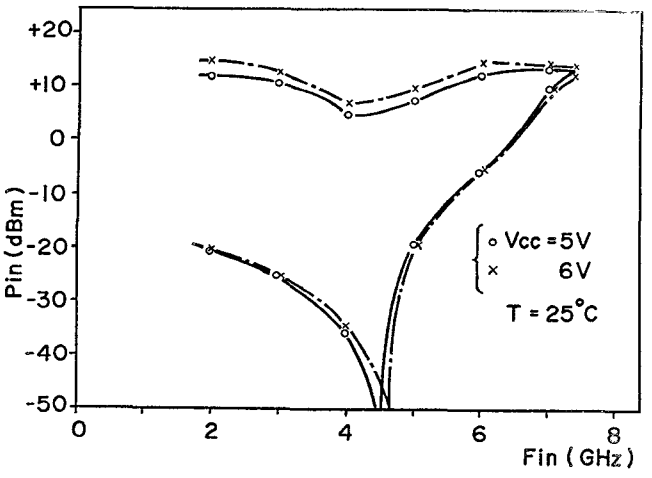

Figure 8. Input frequency (Fin) dependence of input power (Pin) for 1/2 prescaler at Vcc of 5V and 6V.

IV.Application to a frequency divider

The "DNP-Ⅲ" process was applied to 1/2 prescaler. Figure 6 shows equivalent circuit of 1/2 prescaler with master slave T-type flip-flop. Figure 7 shows a microphotograph of 1/2 prescaler chip. The size of the chip was 0.5mm square.

Figure 8 shows the input frequency (Fin) dependence of input power (Pin) for 1/2 prescaler at Vcc of 5V and 6V. Measuring temperature was 25°C. Maximum dividing fequency (Fmax) was 7.3GHz and Icc was 16.6mA at Vcc of 5V. At Vcc of 6V, Fmax of 7.4GHz and Icc of 21.2mA were achieved.

V.Summary and Conclusion

We demonstrated a newly developed "DNP-Ⅲ" process for microwave frequency Si bipolar transistor employing no self-alignment techniques. An NPN transistor with 0.6um width and 0.1um depth emitter achieved f_T of 20GHz and $|S_{21e}|^2$ of 16.4dB at Vce of 3V. At Vce of 5V, f_T is 22GHz and $|S_{21e}|^2$ is 17.1dB.

Maximum dividing frequency of 7.3GHz at Vcc of 5V and 7.4GHz at Vcc of 6V are achieved for 1/2 prescaler IC's employing "DNP-Ⅲ" process.

In addition, NPN transistors formed by "SIC" technique in "DNP-Ⅲ" process achieved f_T of 30GHz and $|S_{21e}|^2$ of 17.5dB at Vce of 3V, and has relatively lower BVcbo and BVceo than those of "DNP-Ⅲ" without "SIC".

Acknoledgement

The authors would like to express their thanks to Mr. Tokanai and Mr. Kitagawa for their continuous support and encouragement. And they also wish to thank Mr. Watanabe and Mr. Ueno for their useful advice and encouragement.

Refernces

(1) S.Konaka, et al.,Ext.Abs. 19th Conf. Solid State Devices and Mater.,pp.331,1987
(2) H.Hamano, et al.,1988 ISSCC Tech. Dig.,pp.18
(3) T.Nakata, et al.,1985 IEEE MTT-S International Microwave Symposium Dig.,pp.55